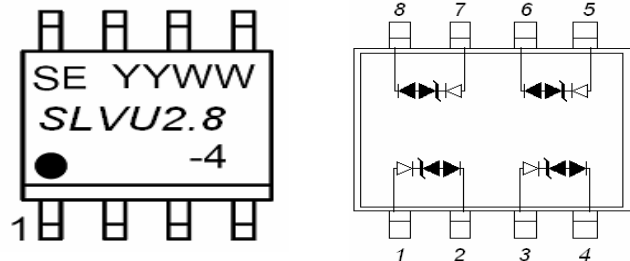




## Description

The SES2V8P8U is in a SOP-8 package and may be used to protect two high-speed line pairs. The “flow-thru” design minimizes trace inductance and reduces voltage overshoot associated with ESD events. The low clamping voltage of the SES2V8P8U minimizes the stress on the protected IC. The component is in accordance to RoHS.



## Features

- 400 W Peak Pulse Power per Line ( $t_p=8/20s$ )
- Protects two line pairs(four lines).
- Low capacitance
- Low Leakage Current
- Low Operating and Clamping Voltages.
- Transient Protection for High Speed Data Lines to
  - IEC61000-4-2(ESD)  $\pm 15kV$ (air),  $\pm 8kV$ (Contact)
  - IEC61000-4-4(EFT) 40A(5/50ns)
  - IEC61000-4-5(lightning) 24A(8/20us)

## Applications

- Audio/Video Input
- Personal Digital Assistant(PDA)
- Ethernet – 10/100/1000 Base T
- WAN/LAN Equipment
- Desktops, Servers, Notebooks & Handhelds, base stations Laser Diode Protection

## Electrical Parameters

Part Number *	$V_{RWM}$ (V)	minimum $V_{BR}$ (V) @ $I_T=1mA$	minimum $V_{SB}$ (V) @ $I_{SB}= 50mA$	maximum $V_C$ (V) @ $I_P= 2A$	maximum $V_C$ (V) @ $I_{pp}=24 A$	maximum $I_D$ ( $\mu A$ ) @ $V_{RWM}$	Typical $C_o$ (pF) @0V,1MHZ
SES2V8P8U	2.8	3.0	2.8	6.5	18	1.0	3.5

## Thermal Consideration

Package SOP-8	Symbol	Parameter	Value	Unit
	$T_J$	Operating Junction Temperature	-55 to +150	$^{\circ}C$
	$T_S$	Storage Temperature Range	-55 to +150	$^{\circ}C$
	$P_{PK}$	Peak Pulse Power ( $t_p = 8/20\mu s$ )	400	W



### Typical Characteristics

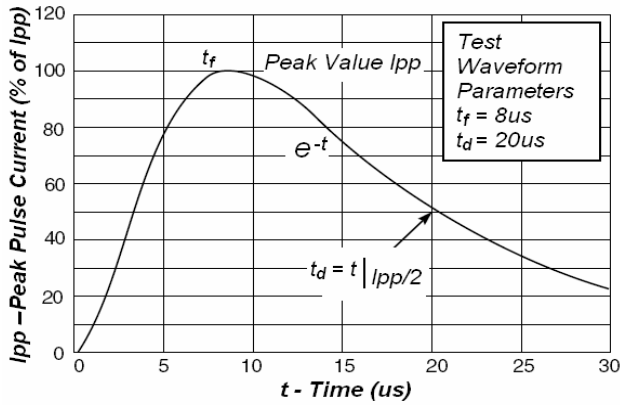


Fig1. Pulse Waveform

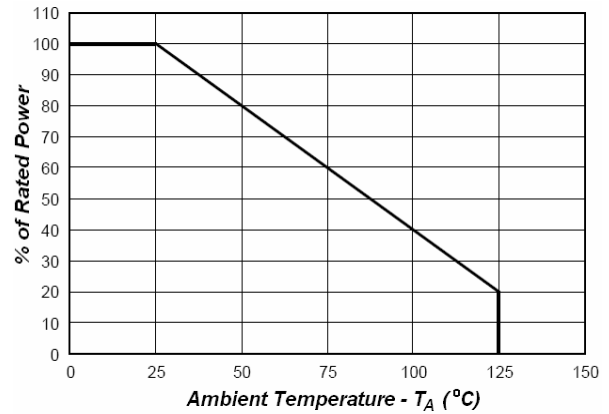


Fig2. Power Derating Curve

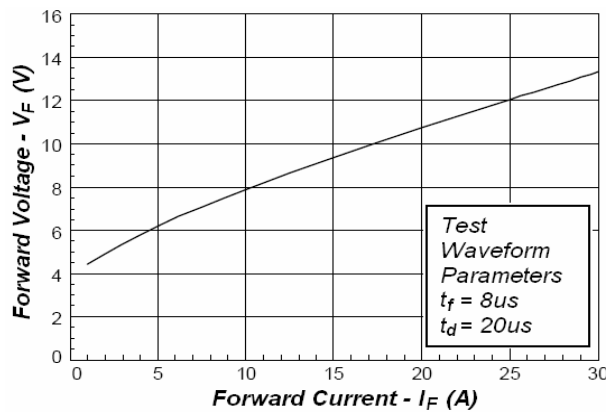


Fig3 Forward Voltage vs. Forward Current

### Application Note:

Electronic equipment is susceptible to damage caused by Electrostatic Discharge (ESD), Electrical Fast Transients (EFT), and tertiary lightning effects. Knowing that equipment can be damaged, the SES2V8P8U was designed to provide the level of protection required to safe guard sensitive equipment. This product can be used in different configurations to provide a level of protection to meet unidirectional line requirements as well as bidirectional requirements either in a common-mode or differential-mode configuration.



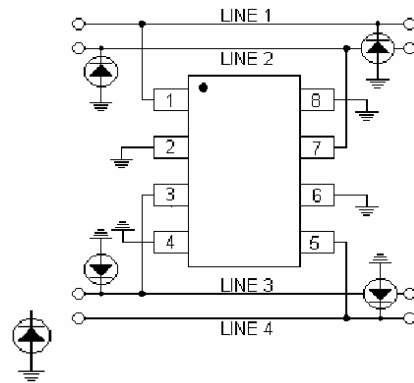
### Configuration Diagram

#### Unidirectional Common-Mode Protection (Figure 5)

The SES2V8P8U provides up to four lines of protection in a common-mode configuration as depicted in figure 5.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 7
- Line 3 is connected to Pin 3
- Line 4 is connected to Pin 5
- Pins 2, 4, 7 and 8 are connected to ground



External diode to ground is a low capacitance diode of less than 10PF

Fig5.

#### Bidirectional Common-Mode Protection (Figure 6)

The SES2V8P8U provides up to two lines of protection in a common-mode configuration as depicted in figure 6.

Circuit connectivity is as follows:

- Line 1 is connected to Pins 1 & 8
- Line 2 is connected to Pins 4 & 5
- Pins 2, 3, 6, and 7 are connected to ground

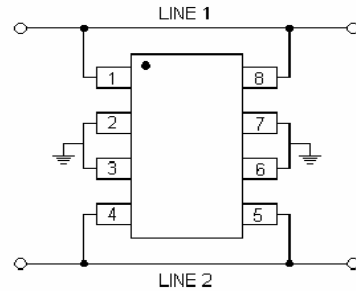


Fig6.

#### Bidirectional differential-Mode Protection (Figure 7)

The SES2V8P8U provides up to two-line pairs of protection in a differential-mode configuration as depicted in figure 7.

Circuit connectivity is as follows:

- Line Pair 1 is connected to Pins 1 & 2
- Line Pair 1 is connected to Pins 7 & 8
- Line Pair 2 is connected to Pins 3 & 4
- Line Pair 2 is connected to Pins 5 & 6

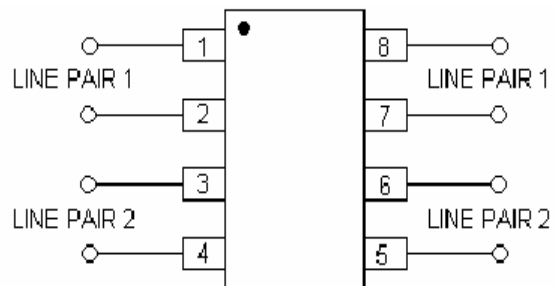


Fig7.

#### Circuit Board Layout Protection

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.