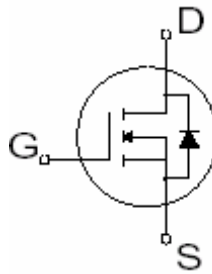


- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



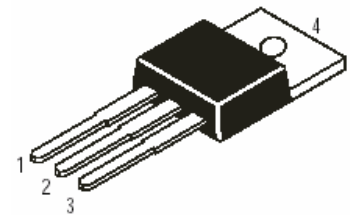
$$V_{DSS} = 600V$$

$$I_{D25} = 9.5A$$

$$R_{DS(ON)} = 0.73 \Omega$$

### Description

StarMOS is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1-Gate  
Pin2-Drain  
Pin3-Source

### Application

- Switching application

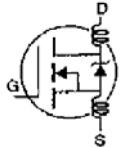
### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}@10V$	9.5	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}@10V$	5.7	
$I_{DM}$	Pulsed Drain Current ①	38	
$P_D@T_C=25^\circ C$	Power Dissipation	156	W
	Linear Derating Factor	1.25	W/°C
$V_{GS}$	Gate-to-Source Voltage	±30	V
$E_{AS}$	Single Pulse Avalanche Energy ②	700	mJ
$I_{AR}$	Avalanche Current ①	9.5	A
$E_{AR}$	Repetitive Avalanche Energy ①	15.6	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	°C
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf.in(1.1N.m)	

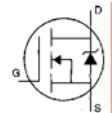
### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	0.8	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62.5	

**Electrical Characteristics @T<sub>J</sub>=25 °C(unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	600	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp.Coefficient	—	0.7	—	V/°C	Reference to 25°C, I <sub>D</sub> =250μA
R <sub>DS(on)</sub>	Static Drain-to-Source On-resistance	—	0.6	0.73	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =4.75A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	—	8.0	—	S	V <sub>DS</sub> =40V, I <sub>D</sub> =4.75A
I <sub>DSS</sub>	Drain-to-Source Leakage current	—	—	1	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V
		—	—	10		V <sub>DS</sub> =480V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C
I <sub>GSS</sub>	Gate-to-Source Forward leakage	—	—	100	nA	V <sub>GS</sub> =30V
	Gate-to-Source Reverse leakage	—	—	-100		V <sub>GS</sub> =-30V
Q <sub>g</sub>	Total Gate Charge	—	44	57	nC	I <sub>D</sub> =9.5A
Q <sub>gs</sub>	Gate-to-Source charge	—	6.7	—		V <sub>DS</sub> =480V
Q <sub>gd</sub>	Gate-to-Drain("Miller") charge	—	18.5	—		V <sub>GS</sub> =10V
t <sub>d(on)</sub>	Turn-on Delay Time	—	23	55	nS	V <sub>DD</sub> =300V
t <sub>r</sub>	Rise Time	—	69	150		I <sub>D</sub> =9.5A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	144	300		R <sub>G</sub> =25Ω
t <sub>f</sub>	Fall Time	—	77	165		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	1570	2040	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	166	215		V <sub>DS</sub> =25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	18	24		f=1.0MHz

**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	9.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	38		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.4	V	T <sub>J</sub> =25°C, I <sub>S</sub> =9.5A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	420	—	nS	T <sub>J</sub> =25°C, I <sub>F</sub> =9.5A
Q <sub>rr</sub>	Reverse Recovery Charge	—	4.2	—	nC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> + L <sub>D</sub> )				

## Notes:

- ① Repetitive rating; pulse width limited by max.junction temperature
- ② L = 14.2mH, I<sub>AS</sub> =9.5 A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C

- ③ I<sub>SD</sub> ≤ 9.5A, di/dt ≤ 200A/μS, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 25°C

- ④ Pulse width ≤ 300 μS; duty cycle ≤ 2%